Vzense DCAM10 TOF Camera Module Hardware User Manual

Revision History

version number	Author
R01_20190701	Peter Liu, Jerry Deng, Sky Guo
R02_20190720	Sky Guo

1 Overview

Welcome to the product user manual for the Vzense TOF Camera Moduel(DCAM10). The DCAM10 is a 3D camera hardware module, developed by Vzense, which uses time-of-flight (TOF) technology to capture depth information while recording imagery. The DCAM10 using MIPI and I2C interface is designed for embedded platform in wide range of environments while providing high-precision depth information.

2 Features

- TOF (Time of flight) Camera technology
- Can output Depth and IR Image
- Field of View (FOV):

  Horizontal: 58° (Customizable)

  Vertical: 43.84°
- Lens TV Distortion: -6.42%
- Depth Camera support image resolution:

  Depth only: 640*480

  IR only: 640*480

  Depth&IR: 640*960
- Image transfer rate: up to 30FPS
- Output formats: 12-bit RAW
- Output interface: 1- or 2-lane MIPI

  1- lane MIPI serial output: 270Mbps

2- lane MIPI serial output: 135Mbps

- Two-wire serial bus control
- Power supply:

  Typical VDD: 3.0V - 5.5V
- Temperature range:

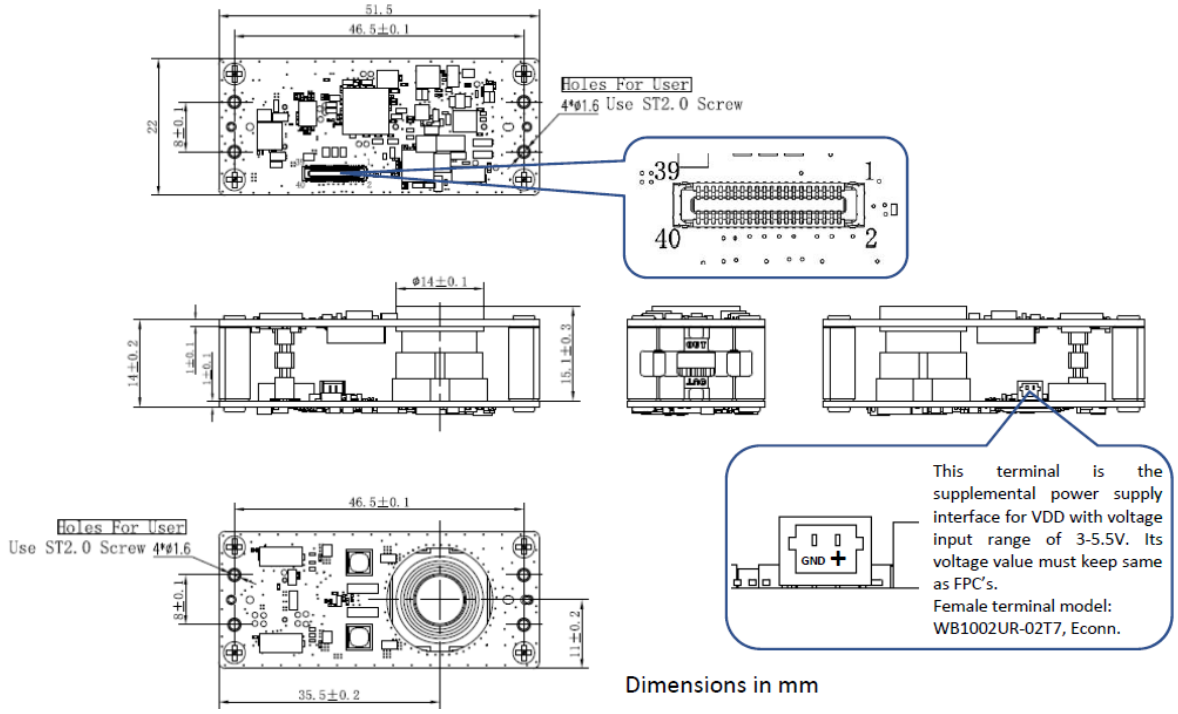
  operating: -10℃ to 50℃

  stable: 0℃ to 50℃

  storage: -40℃ to 70℃
- Accuracy: <1%
- Support OS: Android / Linux / FreeRTOS
- Vzense Depth Sensor Software Support: driver demo code, image algorithm processor lib
- Switchable short and long range modes
- Illumination: 850nm / 940nm, VCSEL
- IR VCSEL security level is Class 1
- Power consumption: <2W Ref.(3 meter)

3 Camera Hardware Information

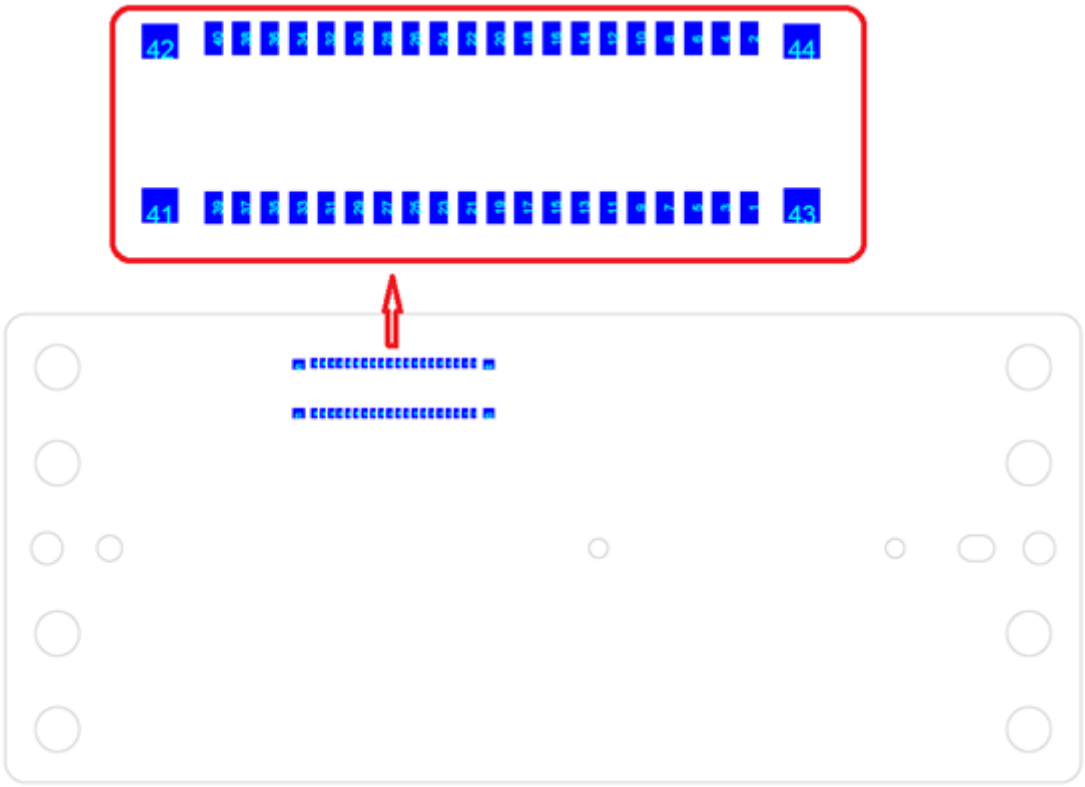
3.1 Module Mechanical Dimension



Dimensions in mm

3.2 Pin Configuration

Layout Top View like below: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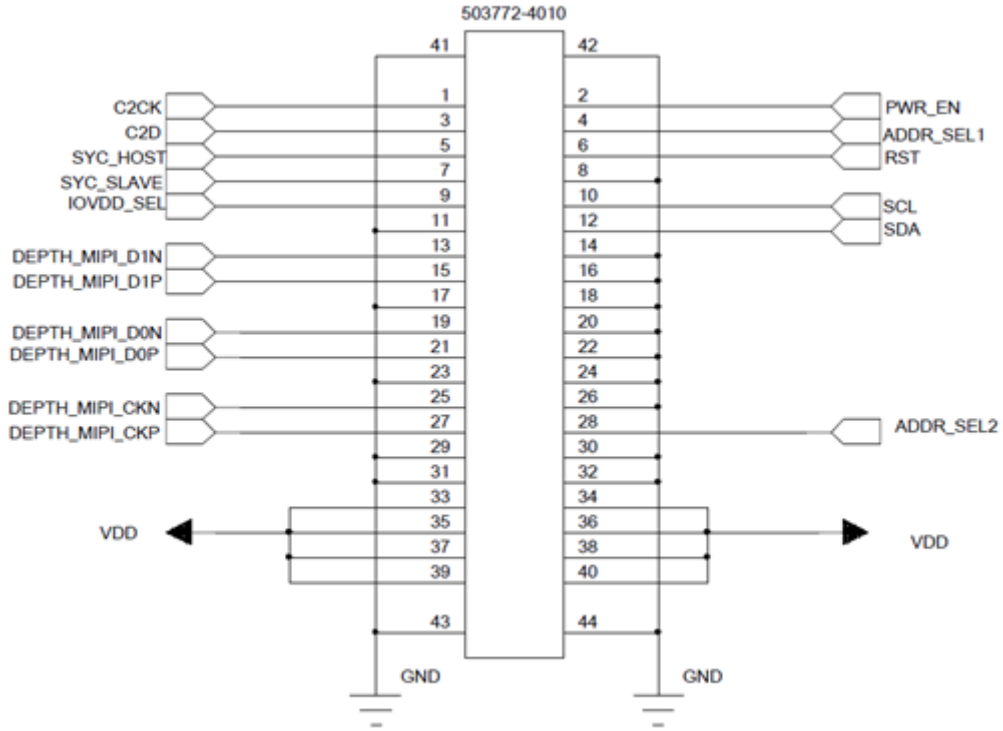
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C2CK
C2D
SYC_HOST
SYC_SLAVE
IOVDD_SEL
DEPTH_MIPI_D1N
DEPTH_MIPI_D1P
DEPTH_MIPI_D0N
DEPTH_MIPI_D0P
DEPTH_MIPI_CKN
DEPTH_MIPI_CKP
VDD
GND
PWR_EN
ADDR_SEL1
RST
SCL
SDA
ADDR_SEL2
VDD
GND

Pin	Parameter	Type	Discription		Min	Typ	Max	unit
1	C2CK	DI	Module firmware update,			1.8/3.3		V
3	C2D	DIO	Module firmware update			1.8/3.3		V
2	PWR_EN	DI	TOF module power control pin, must keep high when working	VH:	1.2			V
				VL:			0.4	V
4	ADDR_SEL1	DI	I2C address set	VH:	0.85		6	V
				VL:			0.4	V
28	ADDR_SEL2	DI	I2C address set	VH:	0.85		6	V
				VL:			0.4	V
5	SYC_HOST	DO	Synchronize singnal output	Refer to below Note1		1.8/3.3		V
7	SYC_SLAVE	DI	Synchronize singnal intput			1.8/3.3		V
6	RST	DI	Module reset, low or floating available. Effective time of low-level needs more than 10ms		0.9	1.8	1.9	V
					0		0.7	V
8,11,14,16,17,18,20,22,23,24,26,29,30,31,32	GND	P	GND					
9	IOVDD_SEL	DI	IO Voltage level select, Low-1.8V, High-3.3V.Default =Low(pull down 10K)	VH:	1.6	1.8/3.3	3.5	V
				VL:	0		0.4	V
10	SCL	DI	I2C bus			1.8/3.3		V
12	SDA	DIO	I2C bus			1.8/3.3		V
13	DEPTH_MIPI_D1N	DO	MIPI data					
15	DEPTH_MIPI_D1P	DO	MIPI data					
19	DEPTH_MIPI_D0N	DO	MIPI data					
21	DEPTH_MIPI_D0P	DO	MIPI data					
25	DEPTH_MIPI_CKN	DO	MIPI clock					
27	DEPTH_MIPI_CKP	DO	MIPI clock					
33,34,35,36,37,38,39,40	VDD	P	Power		3	5	5.5	V

*P is power, DO is digital output, DI is digital input, DIO is digital input/output, and NC is no connect.

Note:

1. SYC_HOST, SYNC_SLAVE can be used only for multiple TOF modules synchronization application. SYC_HOST as a master signal out, and SYNC_SLAVE as a slave module receive. There are two options to choose when multiple modules will be used synchronously:

1) Master module connects the output signal of SYC_HOST to the I/O1 of CPU, and connect slave module's SYC_SLAVE signal to the I/O2 of CPU. When CPU receives master module's SYC_HOST signal, it will control slave device to synchronize through I/O2.

2) Master module's SYC_HOST is directly connected to slave module's SYC_SLAVE. Each module can be configured as a master or slave module through register.

If don't use SYC_HOST and SYNC_SLAVE pins, they can be floating.

2. 40pin connector model: Molex, 503772-4010.

Durability (mating cycle max): 15-30 times.

3.3 Typical Power Consumption

Range0: 0.35-1.5m: 280mA

Range2: 0.8-4.4m: 540mA

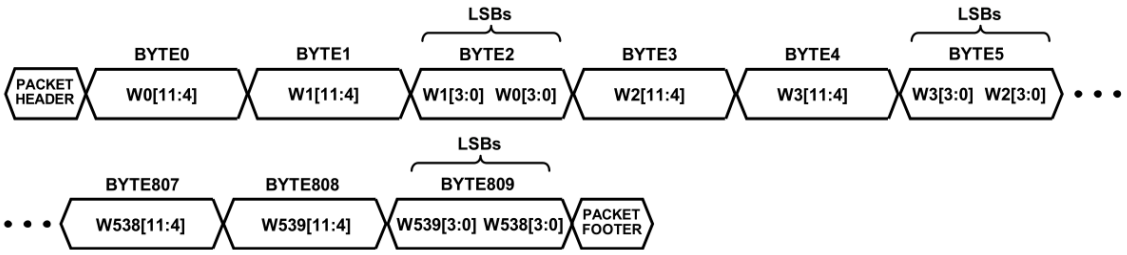
Range5: 1.2-6.2m: 860mA

Test note: VDD=5V@30FPS

3.4 MIPI Interface

TOF module output 12-bit raw data. The MIPI interface can be configured for 1/2-lane via software setting. The one lane configuration can support 270Mbps, the two lanes configuration only can support 135Mbps each lane.

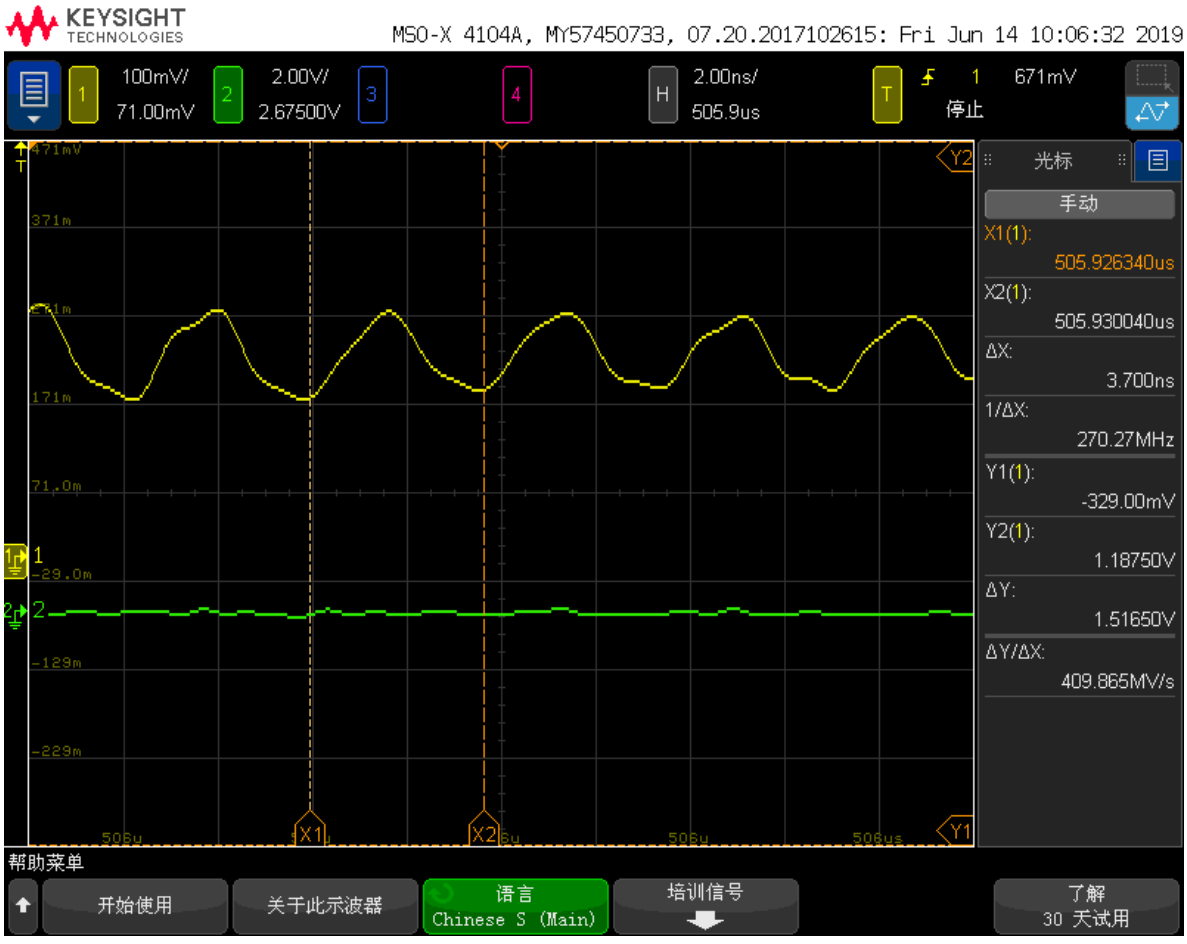
3.4.1 MIPI Raw Data Format



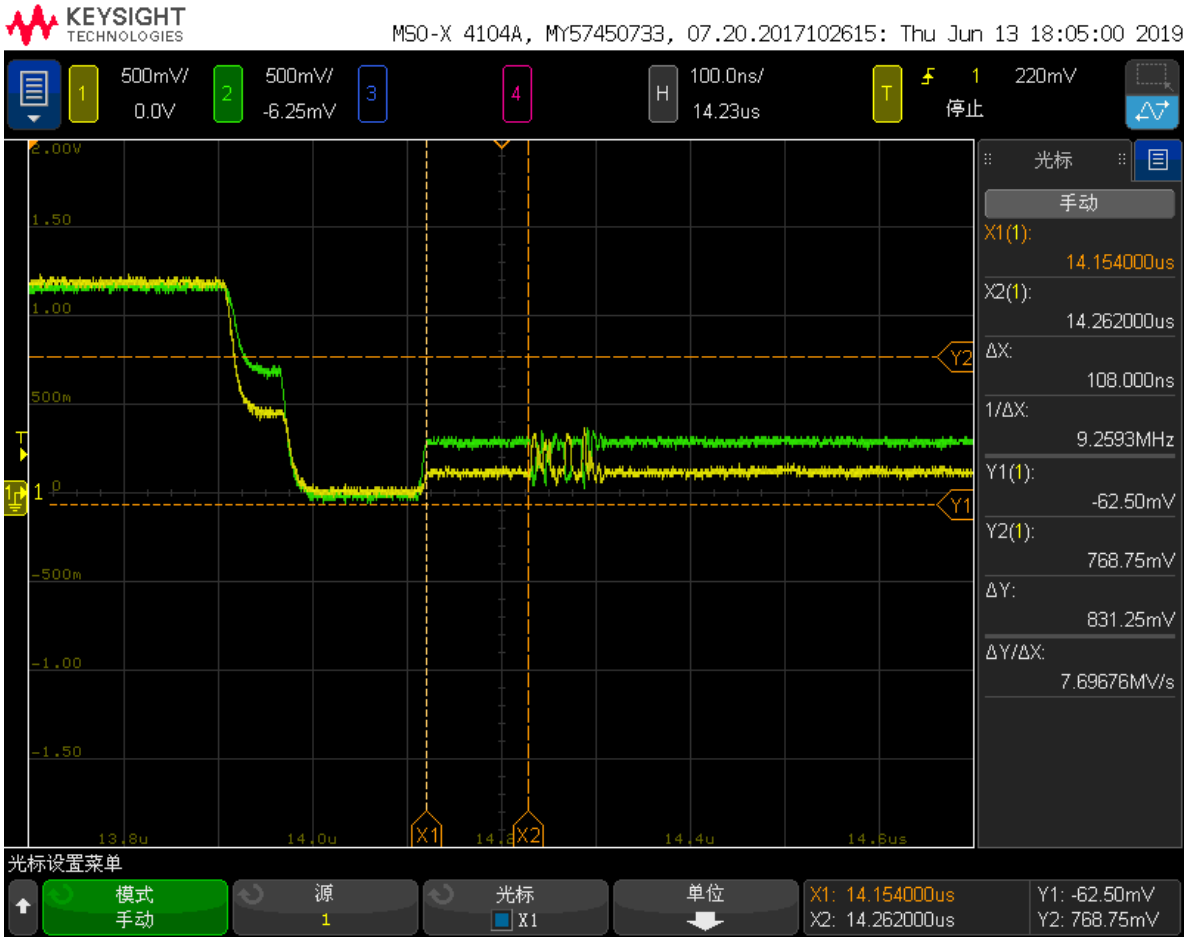
3.4.2 Hardware Waveforms Parameters(1-Lane)

Item	Value
MIPI Clock	270MHz
MIPI Prepare+Zero Time	108.00ns
MIPI High Speed Differential Voltage	200.00mV
MIPI Low Speed Voltage	1.20V

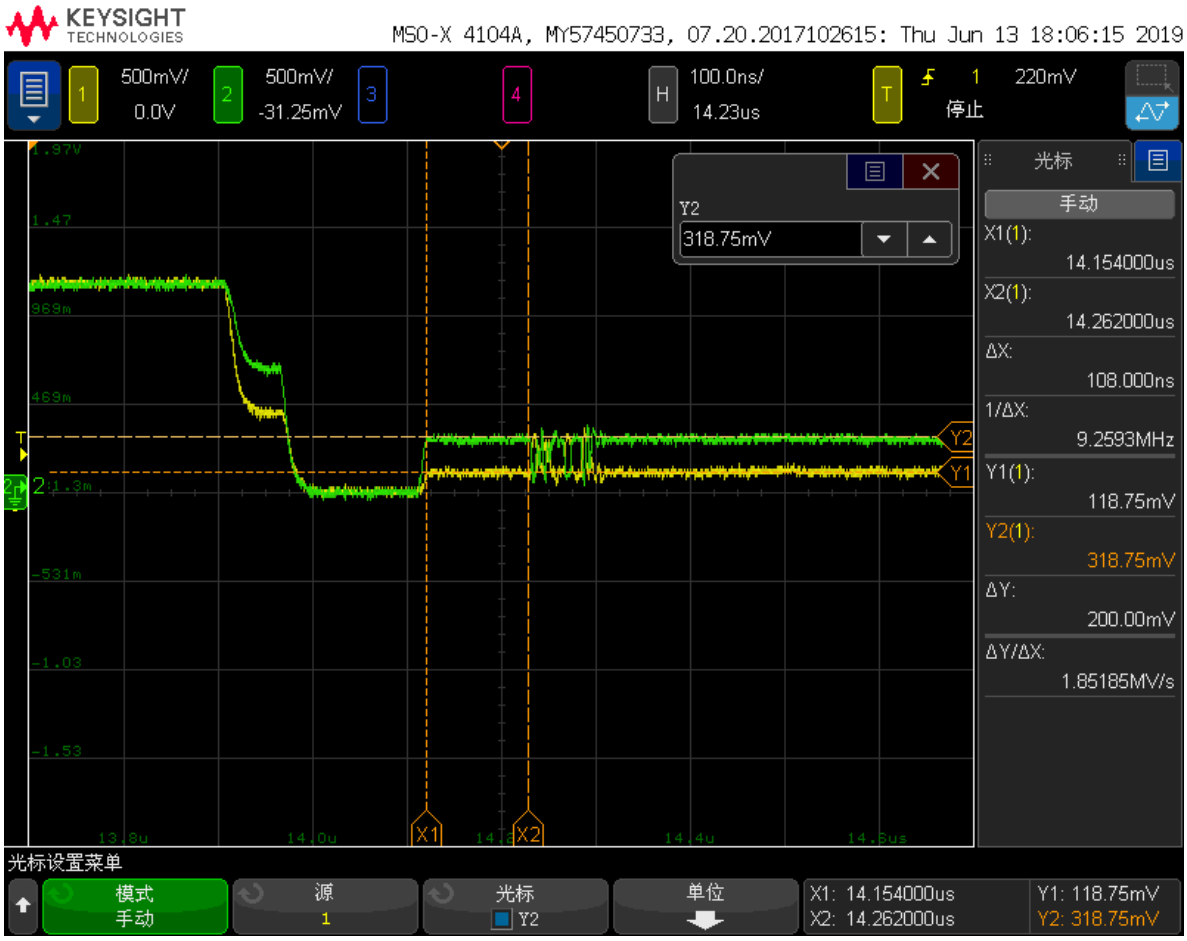
MIPI Clock figure：



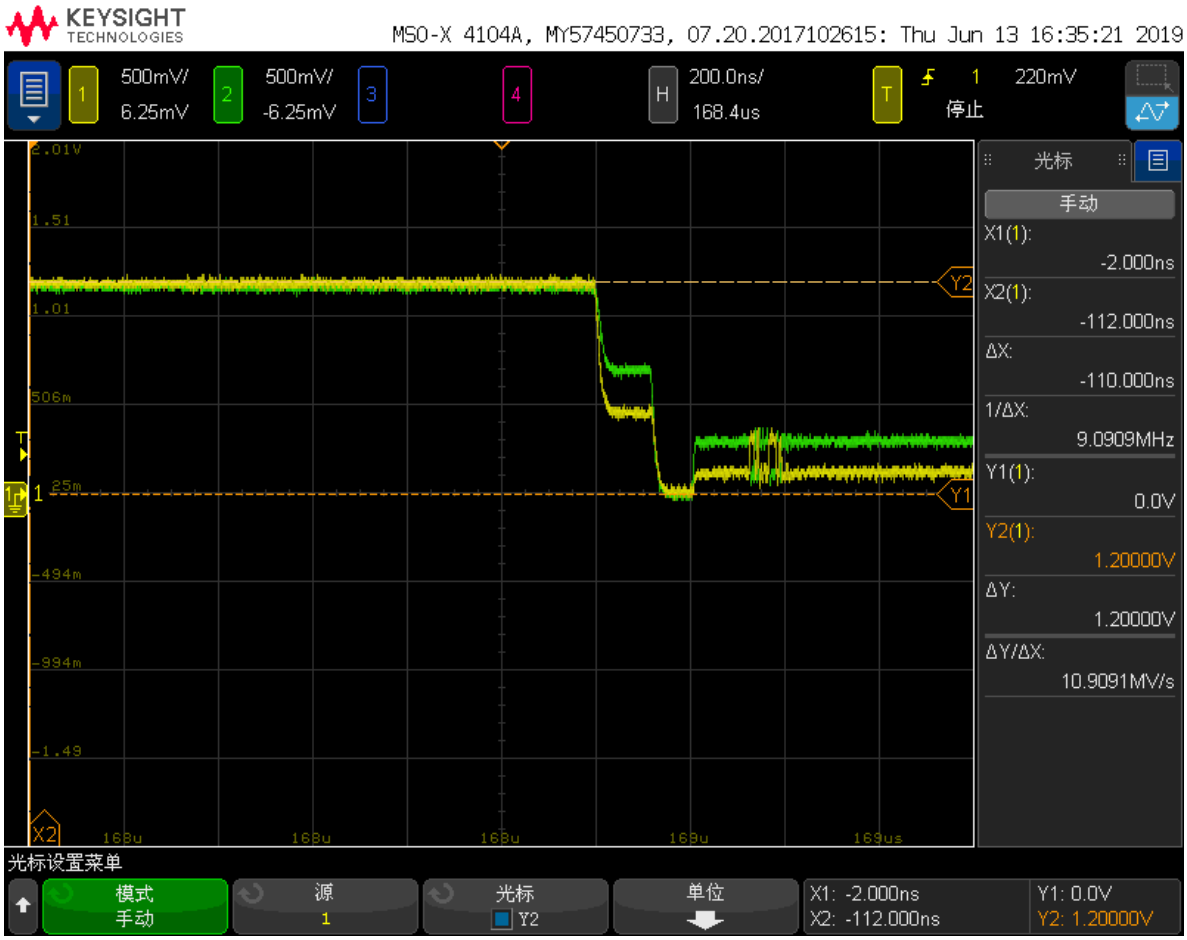
MIPI Prepare+Zero Time figure：



MIPI High Speed Differential Voltage figure：



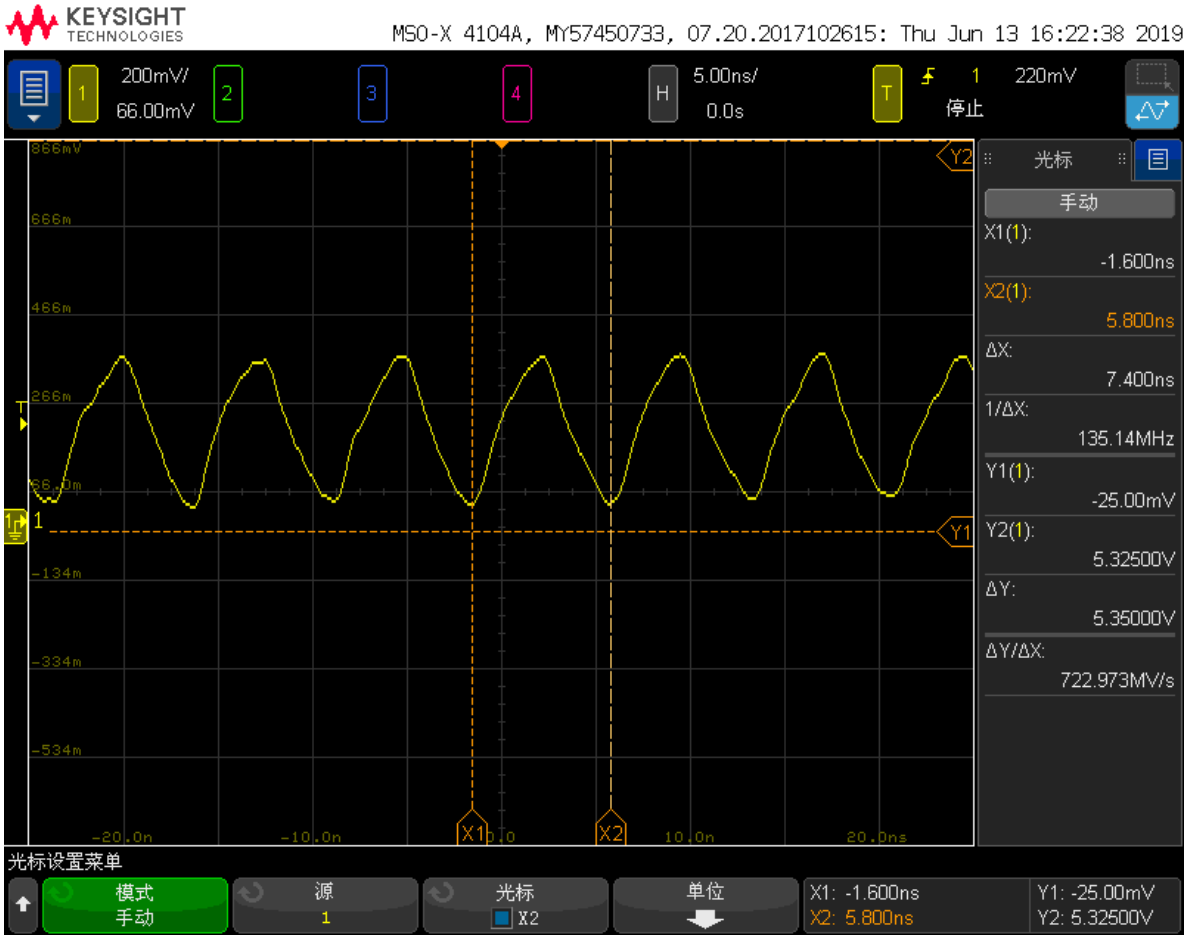
MIPI Low Speed Voltage figure：



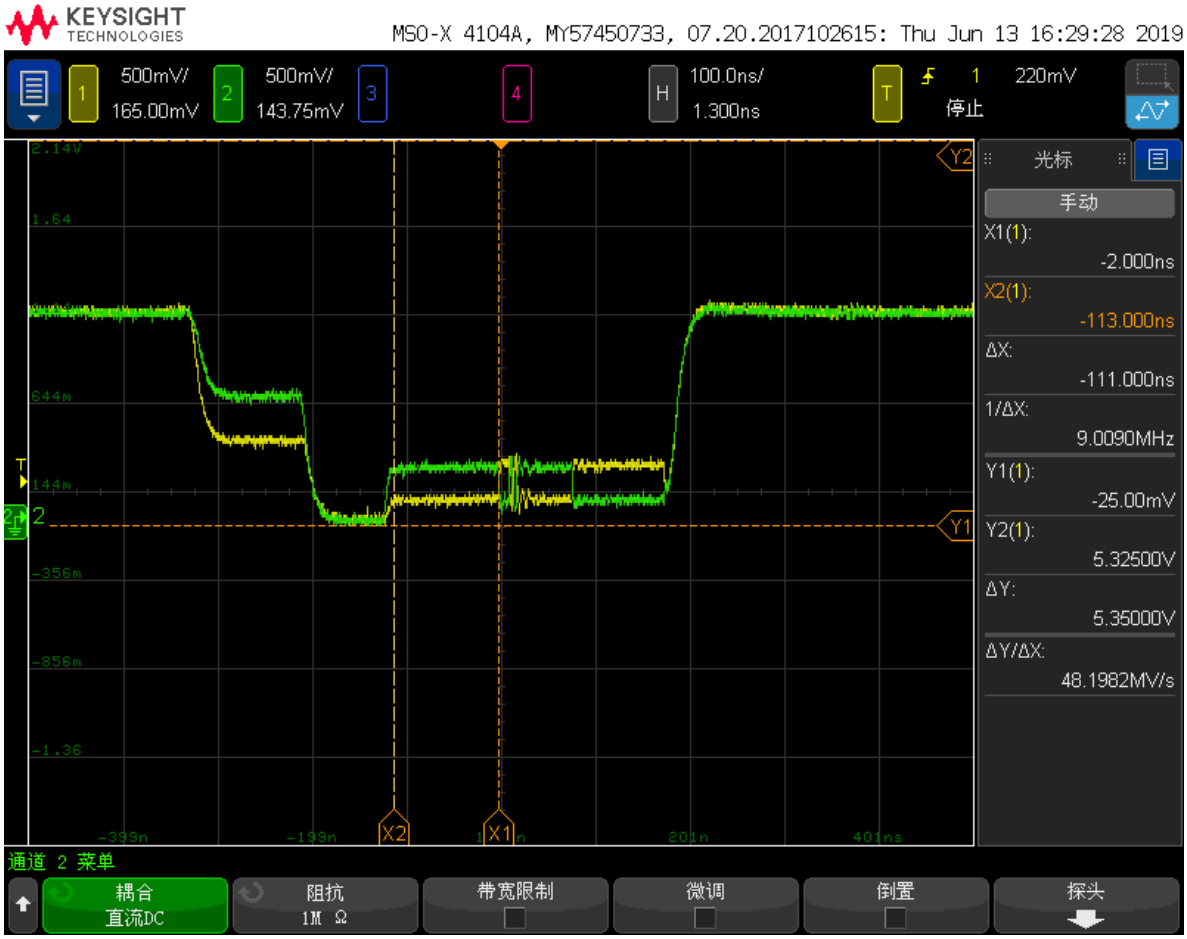
3.4.3 Hardware Waveforms Parameters(2-Lane)

Item	Value
MIPI Clock	135MHz
MIPI Prepare+Zero Time	111.00ns
MIPI High Speed Differential Voltage	200.00mV
MIPI Low Speed Voltage	1.20V

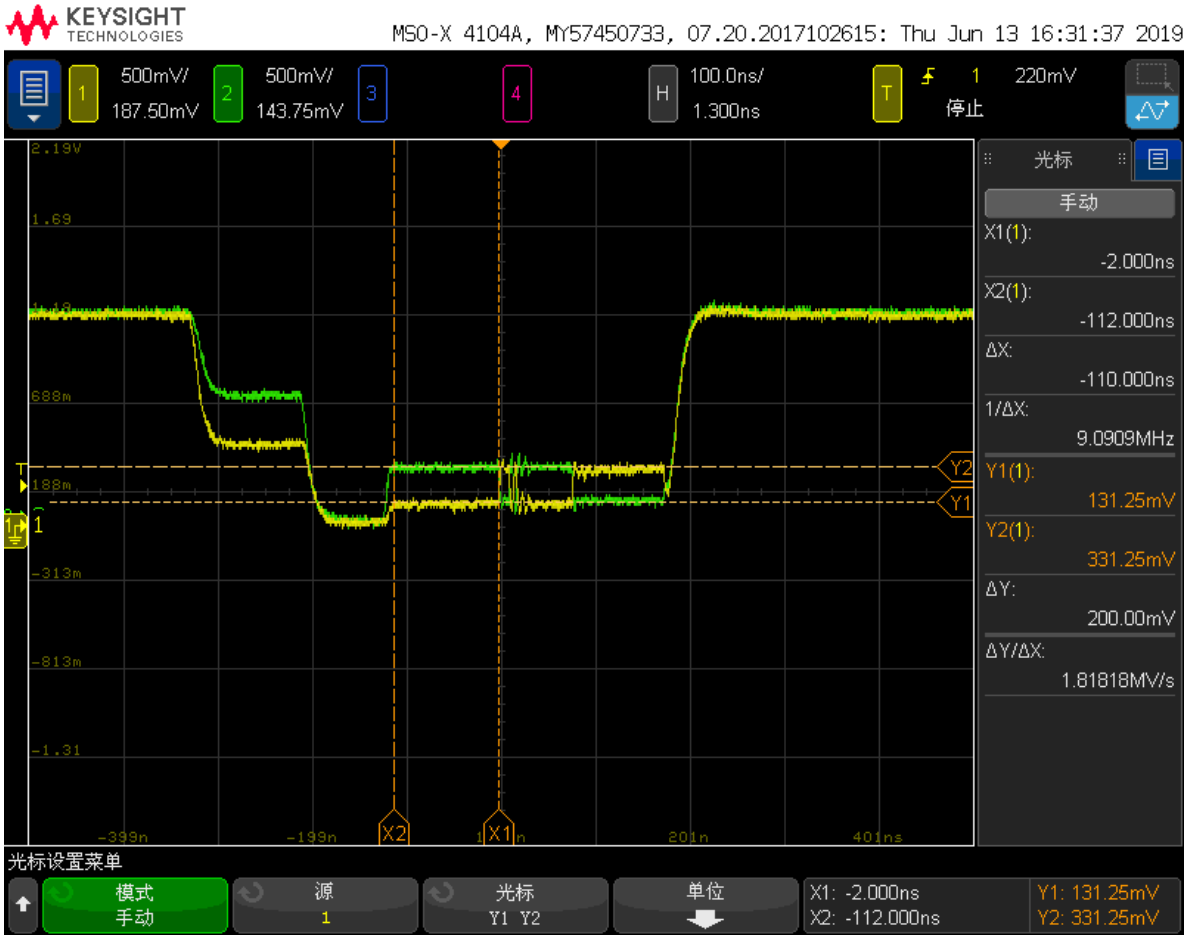
MIPI Clock figure:



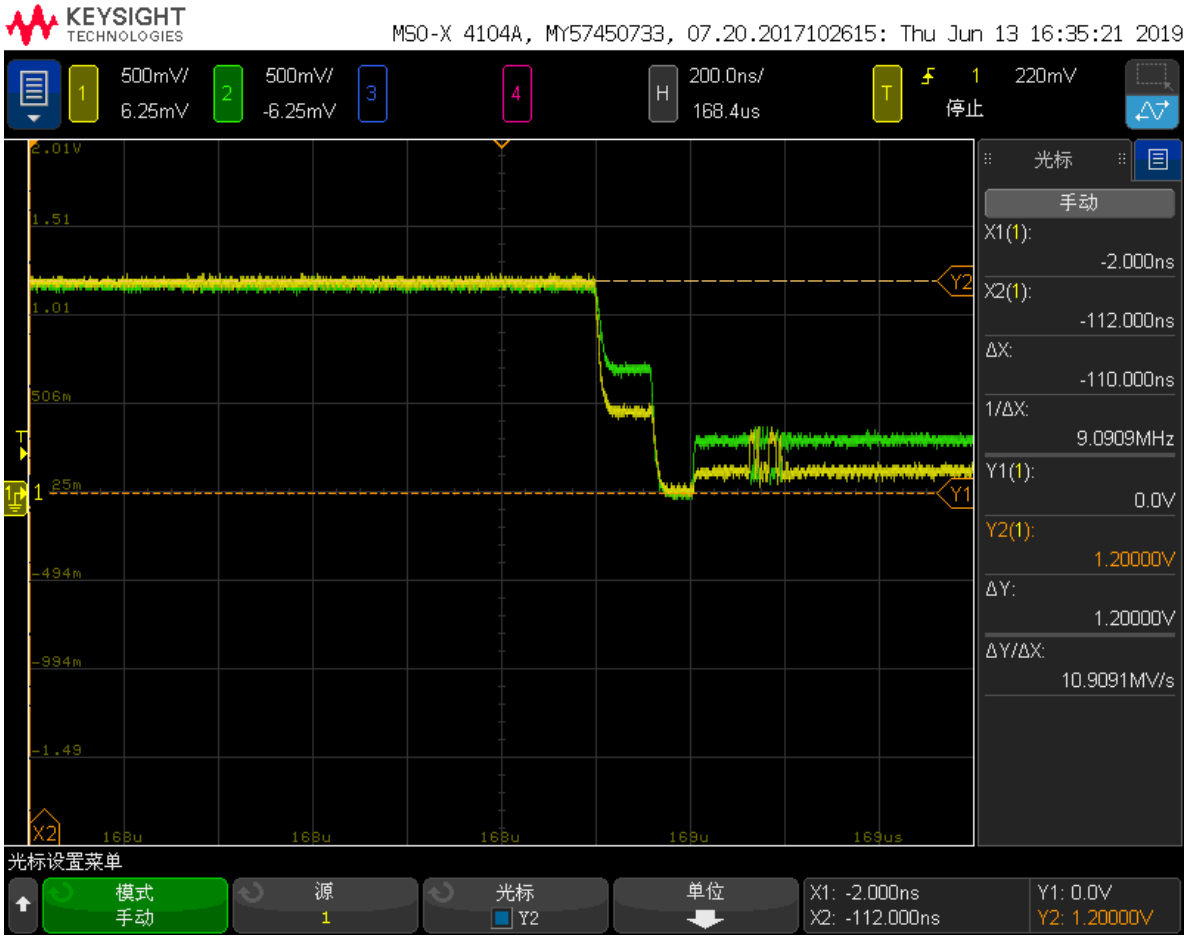
MIPI Prepare+Zero Time figure:



MIPI High Speed Differential Voltage figure:



MIPI Low Speed Voltage figure:



4 DCAM10 Driver Debugging

Vzense DCAM10 is a MIPI interface TOF module, so need to debug the corresponding driver according to the connected platform. Vzense will provide the needed technical document < *Vzense MIPI TOF Camera Module* Software User Manual> contains detailed description for driver debugging, which help engineers quickly complete the drive debugging work.